

M5STACK

M5IOE1 Chip User Manual

V 1.4

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I. Overview

The M5IOE1 is an IO extension management chip that provides fixed IO management, ADC, interrupt and other functions by burning custom IO function firmware to M5Stack.

1. Resource

- (1) 14 GPIOs
- (2) 1 set of I²C interfaces
- (3) Built-in temperature sensor
- (4) 32-byte RAM protected area

2. Function

- (1) 14 GPIOs expansion :
 - 4 channels multiplexed as 12-bit ADC
 - 4 channels multiplexed as PWM
 - 1 channel multiplexed for LED control (RGB565)
- (2) GPIO supports programmable pull-up/down resistors, open-drain / push-pull output, and interrupt polarity control
- (3) Supports reading the built-in temperature sensor and internal reference voltage
- (4) I²C interface supports 100 kHz (default) / 400 kHz modes, configurable address range: 0x6F–0x76
- (5) Supports PWM-based AW8737A control for audio signal amplitude
- (6) Supports driving up to 32 Neopixel RGB LEDs simultaneously

3. Custom firmware pin arrangement

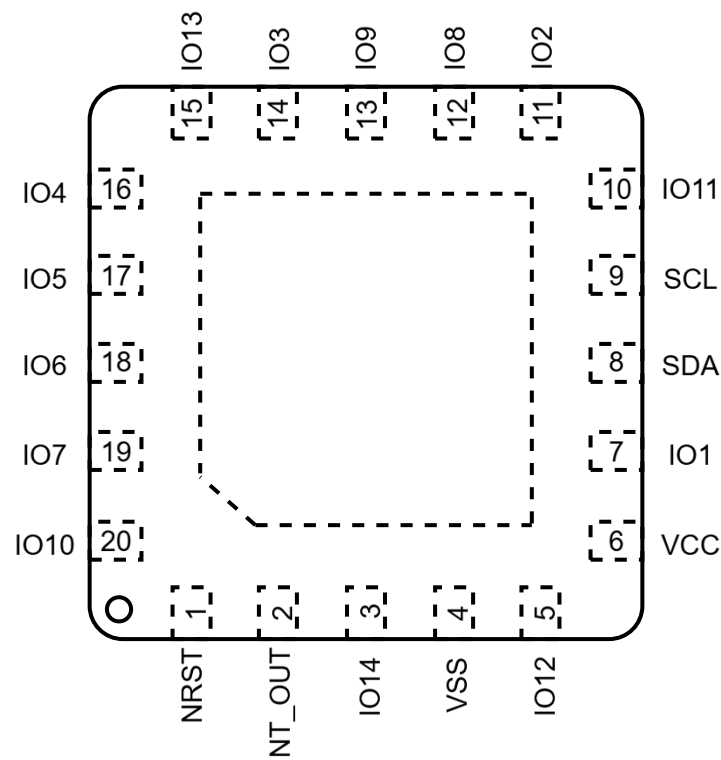




Table 1 Custom Firmware Pin

Pin Num	Pin Name	Pin Type	Pull Up/Down
1	NRST	NRST	none
2	INT_OUT	Interrupt output	none
3	IO14	GPIO	none
4	VSS	VSS	none
5	IO12	GPIO	none
6	VCC	VCC	none
7	IO1	GPIO	none
8	SDA	I ² C	none
9	SCL	I ² C	none
10	IO11	GPIO	none
11	IO2	GPIO	none
12	IO8	GPIO	none
13	IO9	GPIO	none
14	IO3	GPIO	none
15	IO13	GPIO	none
16	IO4	GPIO	none
17	IO5	GPIO	none
18	IO6	GPIO	none
19	IO7	GPIO	none
20	IO10	GPIO	none



II. Pin Definitions

Table 2 Pin Definition

Pin	Description	Default	MUX	Note
IO1	GPIO port 1, configurable I/O	GPIO	-	Interrupt mutually exclusive with IO6
IO2	GPIO port 2, configurable I/O	GPIO	ADC1	Interrupt mutually exclusive with IO3; Interrupt disabled when ADC is enabled
IO3	GPIO port 3, configurable I/O	GPIO	-	Interrupt mutually exclusive with IO2
IO4	GPIO port 4, configurable I/O	GPIO	ADC2	Interrupt disabled when ADC is enabled
IO5	GPIO port 5, configurable I/O	GPIO	ADC3	Interrupt disabled during I ² C idle sleep; Interrupt disabled when ADC is enabled
IO6	GPIO port 6, configurable I/O	GPIO	-	Interrupt mutually exclusive with IO1
IO7	GPIO port 7, configurable I/O	GPIO	ADC4	Interrupt mutually exclusive with IO12; Interrupt disabled when ADC is enabled
IO8	GPIO port 8, configurable I/O	GPIO	PWM2	Interrupt mutually exclusive with IO9; Interrupt disabled when PWM is enabled
IO9	GPIO port 9, configurable I/O	GPIO	PWM1	Interrupt mutually exclusive with IO8; Interrupt disabled when PWM is enabled
IO10	GPIO port 10, configurable I/O	GPIO	PWM4	Interrupt mutually exclusive with IO14; Interrupt disabled when PWM is enabled
IO11	GPIO port 11, configurable I/O	GPIO	PWM3	Interrupt mutually exclusive with IO13; Interrupt disabled when PWM is enabled
IO12	GPIO port 12, configurable I/O	GPIO	SWDIO	Interrupt mutually exclusive with IO7 SWDIO-Disabled by default
IO13	GPIO port 13, configurable I/O	GPIO	SWCLK	Interrupt mutually exclusive with IO11
IO14	GPIO port 14, configurable I/O	GPIO	Neopixel Output	Interrupt mutually exclusive with IO10
INT_OUT	Interrupt output, pulled low when an external interrupt is triggered, pulled high after clearing GPIO_IS	INT Output	-	Open-drain mode, external pull-up resistor required
SDA	I ² C data line	I ² C	-	Open-drain mode, external pull-up resistor required
SCL	I ² C clock line	I ² C	-	Open-drain mode, external pull-up resistor required
NRST	Reset pin	NRST	-	Active-low reset

Note:

1. All GPIO output types default to **open-drain mode**, including Neopixel driving and PWM outputs. If no external pull-up resistor is used, the GPIO must be configured to push-pull mode to operate correctly.
2. I²C address: 0x6F-0x76. The specific address is determined by the voltage level of IO7 (PA6) at power-on. For details, refer to Section 3.6.



III. Register Mapping

Table 3 Register Map

Addr(H)	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
0x00	UID_L	UID[7:0]	—	—	—	—	—	—	—	—
0x01	UID_H	UID[15:8]	—	—	—	—	—	—	—	—
0x02	REV	SW7	SW6	SW5	SW4	SW3	SW2	SW1	SW0	A
0x03	GPIO_M_L	M8	M7	M6	M5	M4	M3	M2	M1	0x00
0x04	GPIO_M_H	RES	RES	M14	M13	M12	M11	M10	M9	0x00
0x05	GPIO_O_L	O8	O7	O6	O5	O4	O3	O2	O1	0x00
0x06	GPIO_O_H	RES	RES	O14	O13	O12	O11	O10	O9	0x00
0x07	GPIO_I_L	I8	I7	I6	I5	I4	I3	I2	I1	—
0x08	GPIO_I_H	RES	RES	I14	I13	I12	I11	I10	I9	—
0x09	GPIO_PU_L	PU8	PU7	PU6	PU5	PU4	PU3	PU2	PU1	0x00
0x0A	GPIO_PU_H	RES	RES	PU14	PU13	PU12	PU11	PU10	PU9	0x00
0x0B	GPIO_PD_L	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	0x00
0x0C	GPIO_PD_H	RES	RES	PD14	PD13	PD12	PD11	PD10	PD9	0x00
0x0D	GPIO_IE_L	IE8	IE7	IE6	IE5	IE4	IE3	IE2	IE1	0x00
0x0E	GPIO_IE_H	RES	RES	IE14	IE13	IE12	IE11	IE10	IE9	0x00
0x0F	GPIO_IP_L	IP8	IP7	IP6	IP5	IP4	IP3	IP2	IP1	0x00
0x10	GPIO_IP_H	RES	RES	IP14	IP13	IP12	IP11	IP10	IP9	0x00
0x11	GPIO_IS_L	IS8	IS7	IS6	IS5	IS4	IS3	IS2	IS1	0x00
0x12	GPIO_IS_H	RES	RES	IS14	IS13	IS12	IS11	IS10	IS9	0x00
0x13	GPIO_DRV_L	DRV8	DRV7	DRV6	DRV5	DRV4	DRV3	DRV2	DRV1	0xFF
0x14	GPIO_DRV_H	RES	RES	DRV14	DRV13	DRV12	DRV11	DRV10	DRV9	0x3F
0x15	ADC_CTRL	BUSY	START	RES	RES	RES	CH2	CH1	CH0	0x00
0x16	ADC_D_L	ADC Data[7:0]	—	—	—	—	—	—	—	—
0x17	ADC_D_H	RES	RES	RES	RES	ADC Data	ADC Data	ADC Data	ADC Data	—
0x18	TEMP_CTRL	TBUSY	TSTART	RES	RES	RES	RES	RES	RES	0x00
0x19	TEMP_D_L	TEMP Data[7:0]	—	—	—	—	—	—	—	—
0x1A	TEMP_D_H	RES	RES	RES	RES	TEMP Data	TEMP Data	TEMP Data	TEMP Data	—
0x1B	PWM1_L	DUTY[7:0]	—	—	—	—	—	—	—	0x00
0x1C	PWM1_H	EN	POL	RES	RES	DUTY	DUTY	DUTY	DUTY	0x00
0x1D	PWM2_L	DUTY[7:0]	—	—	—	—	—	—	—	0x00
0x1E	PWM2_H	EN	POL	RES	RES	DUTY	DUTY	DUTY	DUTY	0x00
0x1F	PWM3_L	DUTY[7:0]	—	—	—	—	—	—	—	0x00
0x20	PWM3_H	EN	POL	RES	RES	DUTY	DUTY	DUTY	DUTY	0x00
0x21	PWM4_L	DUTY[7:0]	—	—	—	—	—	—	—	0x00



Addr(H)	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
0x22	PWM4_H	EN	POL	RES	RES	DUTY	DUTY	DUTY	DUTY	0x00
0x23	I ² C_CFG	RES	INTERNAL_ PU /PD	WAKE _TYPE	SPD	SLEEP3	SLEEP2	SLEEP 1	SLEEP0	0x00
0x24	LED_CFG	RES	REFRESH	LED5	LED4	LED3	LED2	LED1	LED0	0x00
0x25	PWM_FREQ_L	FREQ[7:0]	—	—	—	—	—	—	—	0xF4
0x26	PWM_FREQ_H	FREQ[15:8]	—	—	—	—	—	—	—	0x01
0x27	REF_VOLTAGE_L	REF_V[7:0]	—	—	—	—	—	—	—	—
0x28	REF_VOLTAGE_H	REF_V[15:8]	—	—	—	—	—	—	—	—
0x29	RESET	RESET[7:0]	—	—	—	—	—	—	—	—
0x30- 0x6F	LED_RAM	Neopixel RGB565 Data (32×2Bytes)	—	—	—	—	—	—	—	0x00
0x70- 0x8F	RTC_RAM	Power-off Retention Memory (32B)	—	—	—	—	—	—	—	0x00
0x90	AW8737A PULSE	REFRESH	NUM	NUM	GPIO	GPIO	GPIO	GPIO	GPIO	0x00

Note:

1. RES: Reserved bit
2. Register access range:

I²C Burst supports continuous read and write operations on blocks 0x00-0x2F , 0x30-0x6F , 0x70-0x8F , and 0x90 .

Operations outside these ranges must be performed in multiple steps.

IV. Key Register Description

1. Device Information

(1) UID[15:0] (0x00-0x01):

16-bit factory-programmed unique identifier (read-only)

(2) REV (0x02):

Firmware major version number (read-only).

2. GPIO control (IO1-IO14)

(1) GPIO_M_x (0x03-0x04): Direction Register

- M[n]=0: Input mode
- M[n]=1: Output mode

Default is input mode.

(2) GPIO_O_x (0x05-0x06): Output Register

Output level (only effective when M[n]=1).

(3) GPIO_I_x (0x07-0x08): Input register (read-only)

Real-time input level.

(4) GPIO_PU_x / GPIO_PD_x (0x09-0x0C): Pull-up / Pull-down Control

Table 4 Pull-up / Pull-down Truth Table

PU[n]	PD[n]	Mode
1	0	Pull-up enabled
0	1	pull-down enabled
0	0	No pull-up/down
1	1	No pull-up/down

(5) GPIO_IE_x (0x0D-0x0E): Interrupt Enable

- IE[n]=1: Enable pin interrupt

(6) GPIO_IP_x (0x0F-0x10): Interrupt Polarity

- IP[n]=1: Rising edge/high level trigger
- IP[n]=0: Falling edge/low level trigger

(7) GPIO_IS_x (0x11-0x12): Interrupt Status

- IS[n]=1: Interrupt triggered (write 0 to clear)

(8) GPIO_DRV_x (0x13-0x14): Driver Mode

- DRV[n]=0: Push-pull output
- DRV[n]=1: Open-drain output

Default is open-drain output.

(9) GPIO Configuration Priority:

When a pin is occupied by ADC / PWM / I²C / SWD / Neopixel, the GPIO input/output configuration (GPIO_M_x, GPIO_O_x) becomes invalid.

3. ADC Control (0x15-0x17)**(1) ADC_CTRL (0x15):**

- CH2:0: Channel Selection

000 = Disabled

001 = ADC1 (IO2)

010 = ADC2 (IO4)

011 = ADC3 (IO5)

100 = ADC4 (IO7)).

- START: Write 1 to initiate 12-bit conversion (auto-cleared by hardware)
- BUSY: 1 = Converting; 0 = Complete (read-only)

**(2) ADC_D_x (0x16-0x17):**

12-bit conversion result: ADC_D_H[3:0] (high 4 bits) + ADC_D_L[7:0] (low 8 bits).

4. Temperature Sensor (0x18-0x1A)**(1) TEMP_CTRL (0x18):**

- TSTART: Write 1 to start sampling (auto-cleared by hardware)
- TBUSY: Sampling in progress (read-only)

(2) TEMP_D_x (0x19-0x1A):

12-bit temperature value: TEMP_D_H[3:0] (upper 4 bits) + TEMP_D_L[7:0] (lower 8 bits), unit: °C

5. PWM control (0x1B-0x22)**(1) PWMx_L:**

- DUTY[7:0] : Lower 8 bits of duty cycle

(2) PWMx_H:

- DUTY[11:8]: Upper 4 bits of duty cycle
- EN: Enable bit (1 = Enable PWM).
- POL: Polarity (1 = Active-low; 0 = Active-high).

(3) Duty Cycle Range:

0x000 (0%) to 0xFFFF (≈100%).

(4) Frequency Control:

Configured by PWM_FREQ (0x25–0x26), 16-bit value, unit: Hz.

(5) PWM Configuration :

High and low bytes are stored in two registers and must be written together; otherwise, temporary mismatched duty cycle or frequency may occur.

6. I²C Configuration (0x23)**(1) INTERNAL_PU/PD:** Whether to enable internal pull-up/pull-down functions

- 0 = Enabled
- 1 = Disabled

(2) WAKE_TYPE : Wake-up trigger type

- 0 = Falling edge
- 1 = Rising edge

(3) SPD: I²C speed

- 0 = 100 kHz
- 1 = 400 kHz

**(4) SLEEP[3:0]:** I²C bus idle sleep time

- X = Sleep for X seconds
- 0 = No sleep

7. Neopixel Control**(1) LED_CFG (0x24) :**

- LED5:0: Number of Neopixel LEDs (0-32; 0 = All off).
- REFRESH: Write 1 to immediately refresh LED_RAM data (auto-cleared).

(2) LED_RAM (0x30-0x6F):

64-byte RGB565 data (32 LEDs × 2 bytes), stored sequentially (PIX0_L = 0x30, PIX0_H = 0x37, ..., PIX31_H = 0x6F).

8. RTC Storage (0x70-0x8F)

- RTC_RAM: 32-byte RAM retention area (can store counters, calibration parameters, etc.).

9. Reference Voltage (0x27-0x28)

- REF_VOLTAGE: 16-bit reference voltage value for converting ADC values to actual voltage, unit: mV.

10. Factory Reset (0x29)

- RESET: Used to restore factory configuration; write 0x3A to trigger.

11. AW8737A PULSE**(1) PULSE_CTRL (0x90): AW8737A Pulse Trigger Register**

- REFRESH (bit 7)
 - 1: Immediately refresh and execute pulse configuration
 - 0: Do not refresh, wait for next trigger.

(2) NUM[1:0] : Number of Pulses

Value range: 0-3, actual output: 0-3 pulses.

Set the appropriate number of pulses as needed.

(3) GPIO[4:0] : Target GPIO Selection

Value range: 0 ~ 13, corresponding to hardware GPIO1 ~ GPIO14.

The specified GPIO will be used as the output pin for the pulse signal.

Note :

1. After pulse configuration is successful, the corresponding GPIO is automatically set to output mode and outputs the configured pulses.
2. GPIO outputs default to open-drain mode. External pull-up resistors are required for normal output; otherwise, configure the GPIO to push-pull mode.



12. Interrupt Mutual Exclusion

Table 5 Interrupt Mutual Exclusion Groups

Pin Group	Mutual Exclusion Description
IO1 & IO6	Interrupts cannot be enabled simultaneously
IO2 & IO3	Interrupts cannot be enabled simultaneously
IO7 & IO12	Interrupts cannot be enabled simultaneously
IO8 & IO9	Interrupts cannot be enabled simultaneously
IO10 & IO14	Interrupts cannot be enabled simultaneously
IO11 & IO13	Interrupts cannot be enabled simultaneously

Note:

1. When ADC/PWM functions are enabled, interrupts on the corresponding pins are automatically disabled.
2. When I²C idle sleep is enabled, interrupts on the corresponding pin (IO5) are automatically disabled.

V. Additional Features

1. ADC Conversion Flow

Write ADC_CTRL to select the channel and start (START=1) → Wait for BUSY=0 → Read ADC_D_H/L

2. PWM Output

Duty cycle = (DUTY[11:0] / 0xFFFF) × 100%, frequency is configured by the PWM_FREQ register.

3. LED Control

Set LED count (LED_CFG[5:0]) → Write LED_RAM (RGB565 format) → Trigger REFRESH = 1

4. I²C Idle Sleep

Configure SLEEP[3:0] to set idle sleep duration; 0 = No sleep. Note that when PWM is enabled, I²C idle sleep is disabled.

5. I²C Address Configuration

At power-on, the device samples the voltage on IO7 (PA6). The I²C address is determined according to the following table.

Table 6 Voltage vs. I²C Address Mapping

Voltage Range	I ² C Address
Floating	0x6F-0x76
0mV-412.5mV	0x6F
412.5mV-825mV	0x70
825mV-1237.5mV	0x71
1237.5-1650mV	0x72
1650mV-2062.5mV	0x73
2062.5mV-2475mV	0x74
2475mV-2887.5mV	0x75
2887.5mV-3300mV	0x76

Note:

1. To avoid voltage fluctuation issues, **do not set the voltage at boundary values**.
2. If the pin is floating, the address will be randomly assigned; therefore, do not leave IO7 floating at power-on.



Appendix

Firmware Modification History		
Version	Date	Change Description
HW:1 / SW:1	7/11/2025	Initial version
HW:1 / SW:2	7/30/2025	1. Added configuration to the protocol for I2C idle sleep wake-up method and whether to enable/disable internal pull-up/pull-down switches. 2. Modify P
HW:1 / SW:3	9/5/2025	1. Configuring the PWM pin as AF will introduce dead reckoning (OD), affecting register consistency. Configuring the PWM pin as AF allows for complete I/O configuration. 2. Pins 1-PC0 maintain NRST function; low level resets the device. Modify the corresponding option word to check. 3. Added address configuration function to Pin19-PA6-IO7, dividing 0-3.3V into 8 levels, for a total of 8 addresses, namely 0x6F-0x76.
HW:1 / SW:4	11/3/2025	1. Added pulse width modulation function to AW8737A 2. Update firmware to version V4
SW:A	11/25/2025	1. Update firmware version to A (ASCII) 2. Remove hardware version

Document Revision History		
Version	Date	Change Description
1	7/15/2025	Initial version
1.1	7/30/2025	1. Update firmware to version V2 2. Revised some technical details.
1.2	9/5/2025	Update firmware to V3
1.3	11/3/2025	Update firmware version to V4
1.4	11/25/2025	1. Update firmware version to A (ASCII) 2. Remove hardware version